Migrating from a 440ZX-66 AGPset to a 440BX AGPset in a Celeron™ Processor Design

Application Note

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Application Note

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1.0 Introduction

This application note outlines the differences between the Intel® 440ZX-66 AGPset and the Intel 440BX AGPset. Design considerations are included for designing a system that uses the Intel 440ZX-66 AGPset but also provides an easy migration path to the Intel 440BX AGPset.

Intel 440ZX-66 AGPset is not an embedded product and will not be supported for the longer embedded lifecycle. As such, when designing with the 82443ZX Host Bridge/Controller, designers should plan the design with a future migration to the 82443BX Host Bridge/Controller in mind. The designers should also validate their 82443ZX Host Bridge/Controller design with 82443BX Host Bridge/Controller to smooth migration in the future.

2.0 Differences Between the Intel® 440ZX-66 AGPset and the Intel® 440BX AGPset

The Intel® 440BX AGPset includes the 82443BX Host Bridge/Controller and the 82371EB PIIX4E for the I/O subsystem. The Intel 440ZX-66 AGPset also uses the 82371EB PIIX4E for the I/O subsystem but includes the 82443ZX Host Bridge/Controller. The 82443ZX Host Bridge/ Controller is equivalent in all respects to the 82443BX with the exceptions noted below. All 82443BX Application Notes, Design Guides and other documentation apply to the 82443ZX.

The reduced features are:

1. The 82443ZX supports a maximum of 2 DIMM sockets (maximum of 256 Mbytes) while the 82443BX supports a maximum of 3 DIMM sockets (maximum of 512 Mbytes)
2. The 82443ZX does not support registered DIMMs while the 82443BX can provide support for 1 Gbyte of memory using registered DIMMs
3. The 82443ZX supports up to 4 external PCI bus masters (i.e., 4 PREQx#/PGNTx# signal pairs) in addition to the PIIX4E (PHOLD#/PHLDA# signal pair) while the 82443BX supports up to 5 external PCI bus masters in addition to the PIIX4E.
4. The 82443ZX does not support ECC
5. The 82443ZX provides single processor support while the 82443BX can support two processors
6. The 82443ZX does not provide Mobile support
7. The 82443ZX provides support for 66 MHz-only host/DRAM bus frequency while the 82443BX provides support for a maximum 100 MHz host/DRAM bus interface.

The differences in the pinouts of the 82443ZX and the 82443BX are shown in Table 1.

Table 1. 443ZX and 443BX Pinout Differences

Ball Number	82443BX Pin Name	82443BX Pin Type	Equivalent 82443ZX Pin Name[1,2,3]	Relationship to Reduced Features (Listed on Page 5)
AF24	CKE5/CSB7#	O	NC	1
AC23	CKE4/CSB6#	O	NC	1
AD23	CKE3/CSA7#	O	CKE3	1
AE24	CKE2/CSA6#	O	CKE2	1
AE16	CSA5#	O	NC	1
AD15	CSA4#	O	NC	1
AB23	CSB5#	O	NC	1
AC26	CSB4#	O	NC	1
AC12	WEB#	O	NC	1
AA17	SRASB#	O	NC	1
AB13	SCASB#	O	NC	1
AD16	MAB0#	O	NC	1
AC16	MAB1#	O	NC	1
AD17	MAB2#	O	NC	1
AB17	MAB3#	O	NC	1
AE18	MAB4#	O	NC	1
AD19	MAB5#	O	NC	1
AB18	MAB6#	O	STRAP0	1
AB19	MAB7#	O	STRAP1	1
AF20	MAB8#	O	NC	1
AC20	MAB9#	O	STRAP2	1
AB20	MAB10	O	STRAP3	1
AE21	MAB11#	O	STRAP4	1
AD21	MAB12#	O	STRAP5	1
AF22	MAB13	O	NC	1
AE13	DQMB1#	O	NC	1
AD14	DQMB5#	O	NC	1
E9	PGNT4#	O	NC	2
D10	PREQ4#	I	TM2 (PU)	2
AE11	MECC0	I/O	NC	3
AA10	MECC1	I/O	NC	3
AA23	MECC2	I/O	NC	3
AA26	MECC3	I/O	NC	3
AF11	MECC4	I/O	NC	3
AD12	MECC5	I/O	NC	3
AA25	MECC6	I/O	NC	3
Y22	MECC7	I/O	NC	3
AE3	WSC#	O	NC	4
AD4	SUSTAT#	I	NC	6

NOTES:
1. All pins labeled NC are NO CONNECTS and should not be connected on the motherboard
2. All pins labeled (PU) should be connected to a 4.7 K to 10 KΩ pull-up resistor to 3.3 V on the motherboard.
3. All pins labeled STRAPx retain their original MABx and MABx# strapping option function.

Register changes required to implement the 82443ZX device functionality are shown below. These specific register/bit combinations should be set as indicated to support the 82443ZX. Refer to the *Intel® 82440ZX AGPset: 82443ZX Host Bridge/Controller* datasheet and the *82440BX BIOS Specification* for more details.

Table 2. Register Changes to Implement 443ZX Functions

Register Name	Address Offset	Change To
NBXCFG - NBX Configuration Register (Device 0)	50-51h	Bit 31:24 - Note 1 Bit 17 - Note 2 Bit 15 - Note 3 Bit 8:7 - Note 4 Bit 6 - Not Applicable
DRAMC - DRAM Control Register (Device 0)	57h	Bit 4 - Not Applicable
DRB[0:7] - DRAM Row Boundary Registers (Device 0)	60h (DRB0) – 67h (DRB7)	Address 64h-67h - Each should be programmed by the BIOS to the value established for address 63h, the DRB[3] value.
MBSC - Memory Buffer Strength Control Register (Device 0)	69-6Eh	Bit 37:36 - Not Applicable Bit 31:28 - Not Applicable Bit 27:26 - Not Applicable Bit 23:22 - Not Applicable Bit 19:18 - Not Applicable Bit 9:6 - Not Applicable
RPS - SDRAM Row Page Size Register (Device 0)	74h-75h	Bit 15:9 - Not Applicable
SDRAMC - SDRAM Control Register (Device 0)	76h	Bit 4 - Not Applicable
ERRCMD - Error Command Register (Device 0)	90h	Bit 1 - Note 2 Bit 0 - Note 2
ERRSTS0 - Error Status Register 0 (Device 0)	91h	Bit 7:0 - Not Applicable
MBFS - Memory Buffer Frequency Select Register	CA-CCh	Bit 21 - Not Applicable Bit 18:16 - Not Applicable Bit 14 - Not Applicable Bit 12:11 - Not Applicable Bit 4:3 - Not Applicable

NOTES:
1. These bits should all be set to “0” because the 82443ZX does not support ECC.
2. This bit should be set to “0” because the 82443ZX does not support ECC.
3. This bit should be set to “1” for single processor use. The 82443ZX does not support the I/O APIC or dual processors.
4. These bits should be set to “00” because the 82443ZX does not support ECC.

3.0 Migrating from the 440ZX-66 AGPset to the 440BX AGPset in a Celeron™ Processor Design

This section presents considerations for designing an Intel® 440ZX-66 AGPset-based motherboard that will support a future migration to the 440BX AGPset. This discussion is based on information contained in the *Intel® 440BX AGPset Design Guide* (order number 290634) and the *Intel® 440BX PCIset Design Guide Update* (order number 290641).

Note: When none of the additional features of the 82443BX will be used when migrating from an 82443ZX design to an 82443BX design, no changes on the motherboard are required.

3.1 Host Interface Considerations

The host interface on the 82443ZX can support a maximum host/DRAM bus frequency of 66 MHz; the 82443BX supports a 100 MHz host/DRAM bus frequency.

In order to design a 66 MHz 82443ZX host-interface motherboard to be ready for a 100 MHz 82443BX host interface in the future, the guidelines presented in *100MHz GTL+ Layout Design Guidelines for the Pentium II Processors and Intel® 440BX AGPset* (order number 243735) must be adhered to. The 82443ZX design should adhere to the recommended 100 MHz system timing parameters and recommended system flight time specs as defined in the *Intel® 440BX PCIset Design Guide Update* (order number 290641).

3.2 DRAM Interface Considerations

The primary difference in the DRAM interface between the 82443ZX and the 83443BX is in the reduction of the amount of DRAM capacity in the former. This is achieved by the removal of signals necessary for the support the larger capacity in the 82443BX.

Specifically, the second copy of chip selects, row address strobes, column address strobes and Memory Address signals available on the 82443BX are designated as No Connects on 82443ZX. Consequently, the DRAM capacity is reduced by half.

In designing an 82443ZX motherboard (2 DIMMs) with a future migration to an 82443BX (3 or 4 DIMMs) in mind, the second copy of the signals (designated as NCs on the ZX – refer to Table 1) should be connected via a 0Ω resistor as shown in Figures 4-2 and 4-3 in the *Intel® 440BX AGPset: 82443BX Host Bridge/Controller* datasheet (order number 290633). When using an 82443ZX, the 0Ω resistors should be depopulated. Once an 82443BX is used, the 0Ω resistor should be populated. Place the 0Ω resistor as close to the ball on the BGA package as possible to eliminate the generation of stubs when the resistors are depopulated.

3.3 AGP Interface Considerations

There are no differences in the AGP interface between the 82443ZX and the 82443BX. All design guidelines and specifications in the *440BX AGPset Design Guide*, the *AGP Interface Specification* and the *AGP Platform Design Guide* apply equally to both devices.

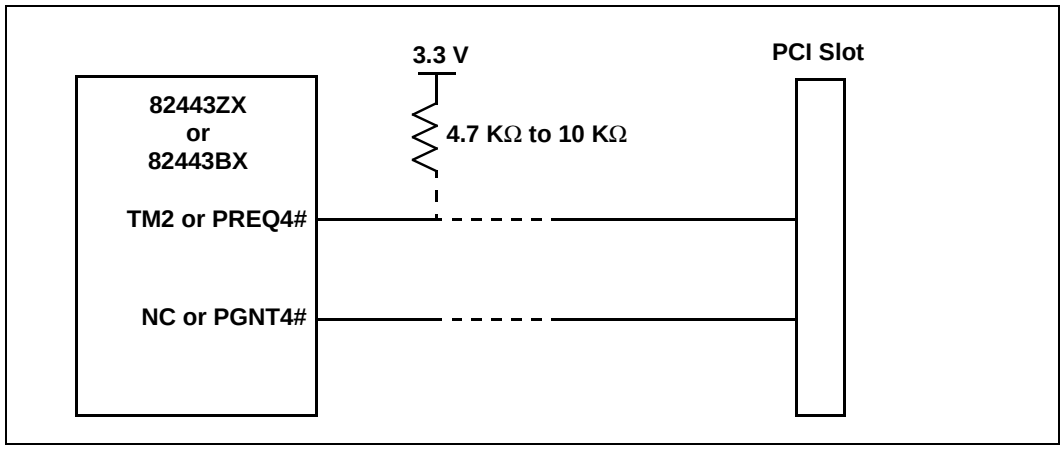
3.4 PCI Interface Considerations

The 82443ZX has one less PREQx#/PGNTx# signal pair then the 82443BX. PGNT4# and PREQ4# on the 82443BX signals are replaced by NC and TM2 signals on the 82443ZX. Thus, on an 82443ZX motherboard design ready for a migration to a 82443BX in the future, the NC will become the output pin PGNT4# while the TM2 will become the input pin PREQ4#.

To remain compliant with the requirements of the 82443ZX while designing for future 82443BX requirements, the NC signal trace should be designed with a 0Ω resistor that is depopulated in a 82443ZX design but populated in a 82443BX design and connects to a PCI slot/device.

By the same token, the TM2 signal on the 82443ZX is required to be pulled up with a 4.7 KΩ to 10 KΩ but should have the option built in to depopulate this resistor and connect a PCI slot/device for a future migration to the 443BX.

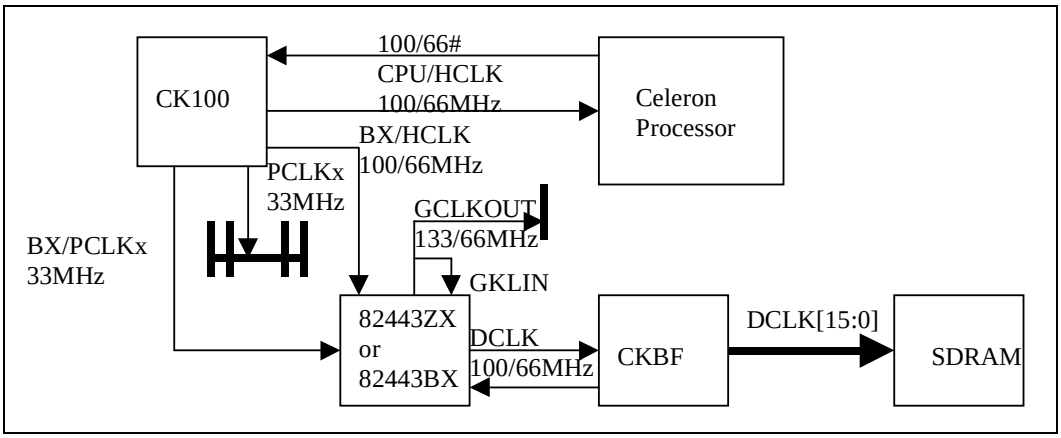
Figure 1. TM2 Signal Pullup Resistor



3.5 System Clocking considerations

The system clocking requirements for both the 82443ZX and the 82443BX are similar. Both systems require the use of CK100 and CKBF compliant clock generators as indicated in the diagram below:

Figure 2. System Clocking Block Diagram



Please refer to the *Intel® Celeron™ processor/ 440BX AGPset Uniprocessor Customer Reference Schematics* and *Intel® Celeron™ processor/ 440ZX AGPset Uniprocessor Customer Reference Schematics* for details of specific connection details for this and other features described in this application note. Contact your Intel Field representative for information about obtaining these documents.

3.6 BIOS Considerations

Existing 82443BX BIOS software may be used without modification with the 82443ZX.